**Verilog code Half subtractor**

**module half\_subtractor(a,b,sub,carry);**

**input a,b;**

**output sub,carry;**

**reg sub,carry;**

**always@(a,b)**

**begin**

**sub= a^b;**

**carry= ~a&b;**

**end**

**endmoudle**

**Testbench of half subtractor**

**module tbhalf\_subtractor();**

**reg a,b;**

**wire sub,carry;**

**integer i;**

**half\_subtractor uut(a,b,sub,carry);**

**initial**

**begin**

**$dumpfile(“dump.vcd”);**

**$dumpvars(1);**

**$monitor($time,”a=%b b=%b sub=%b carry=%b”,a,b,sub,carry);**

**{a,b}=0;**

**for(i=0;i<=4;i=i+1)**

**begin**

**{a,b}=i;**

**#10;**

**end**

**$finish;**

**end**

**endmodule**